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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	13

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/899,573	Applicant(s) ERRATICO, PIETRO	
	Examiner Johannes P Mondt	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-31* is/are pending in the application.

4a) Of the above claim(s) *27-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Amendment B filed 08/28/2002 and entered as Paper No. 12 forms the basis of the present Office Action. In Amendment B Applicant substantially amended all claims pertaining to the invention through substantial amendments of all independent claims 12, 17 and 22. Comments on Remarks by Applicant as included below in "Response to Arguments" are therefore confined to those aspects that are relevant to the new claim set.

Response to Arguments

Applicant's arguments filed 08/28/2002 have been fully considered but they are not persuasive. Although Chang et al admittedly teaches specifically against trenches that do not terminate above a bottom surface of the substrate, Chang et al do teach other embodiments in which this is not the case, such as for instance in Figures 13 and 14, on the basis of which Chang et al can be shown to anticipate the newly described invention. Furthermore, the rejection of claims 12, 13 and 15 as unpatentable of Wada et al stands as being not traversed. Also, while the further limitations of claims 14 (through the newly amended independent claim on which it depends) and 22 force and different interpretation of the limitation on the length of the isolation element with regard to the width of the semiconductor chip said further limitations are obvious over Nakagawa who teach the isolation element or trench separating vertical MOS transistors to have a length substantially equal to the width of the chip, because in Figures 3, 5, and 8 isolation element region 26 extends over the entire chip length.

Motivation for providing an isolation element length equal to the length of portions of a chip that it aims to electrically isolate stems from the very purpose of an isolation element, namely to prevent an electrical conduction path within the chip from one portion to the other. The teaching in this regard by Nakagawa et al can be easily combined with the invention by Chang et al, because all that needs to be done is extend the trench isolation element in the depth direction along substantially the entire width of the semiconductor chip, which does not alter the device or method of making aspects of the device at all. Success of the implementation of the combination can therefore be reasonably expected. In view of this circumstance, claims 14, 22 and claims dependent thereon are herewith rejected under U.S.C. 103(a).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 12-13, 16-19 and 21-24 and 26*** are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al (5,757,081).

With regard to claim 12: Chang et al teach (cf. Figure 14 and column 7, line 57 – column 8, line 22) an integrated structure (cf. title) comprising:

a substrate 10 (cf. column 4, lines 24-27) having first conductivity type (N+);

an epitaxial layer 20 (cf. column 4, lines 24-27) on said substrate having first conductivity type (N-) and conductivity less than said that of said substrate;

first and second regions in said epitaxial layer (any of the P+ regions to the left of 72c and marked 22 and 24 in Figure 1, as first region, and the P-well to the right of 72c in Figure 7 and marked as 38 in Figure 1, as second region, for definiteness), each having a second conductivity type opposite from said first conductivity type (P-type) , said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and second junctions therewith; and:

an isolation element 72c (cf. column 5, line 4) positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as a top surface of said substrate for reducing any injection of current through said epitaxial layer from said first region to said second region when the first junction is directly biased, said isolation element 72c comprising a dielectric material adjacent said epitaxial layer and polycrystalline silicon spaced apart from said epitaxial layer by said dielectric material (cf. column 3, lines 7-15), said isolating element also terminating above a bottom surface of said substrate (cf. Figure 14).

In conclusion: Chang et al anticipate claim 12.

With regard to claim 13: Chang et al teach the integrated structure according to claim 12 wherein said isolating element 72c may surround the power transistor portion 22 and hence the aforementioned first region (cf. column 5, lines 8-13).

With regard to claim 16: the first region as taught by Chang et al comprises a power transistor (cf. column 4, lines 41-45), while it is understood that any power transistor should be able to control any load, i.e., any impedance including inductive load, as described in standard text books such as B. Jayant Baliga, "Modern Power Devices", Krieger Publishing Co., Malabar, Florida, reprint edition 1992, page 377.

With regard to claim 17: Chang et al teach (cf. Figure 14 and column 7, line 57 – column 8, line 22) an integrated structure (cf. title) comprising:

a substrate 10 (cf. column 4, lines 24-27) having first conductivity type (N+);

an epitaxial layer 20 (cf. column 4, lines 24-27) on said substrate having first conductivity type (N-) and conductivity less than said that of said substrate;

first and second regions in said epitaxial layer (any of the P+ regions to the left of 72c and marked 22 and 24 in Figure 1, as first region, and the P-well to the right of 72c in Figure 7 and marked as 38 in Figure 1, as second region, for definiteness), each having a second conductivity type opposite from said first conductivity type (P-type) , said first and second regions extending from a surface of said epitaxial layer opposite

said substrate into said epitaxial layer to form respective first and second junctions therewith; and:

an isolation element 72c (cf. column 5, line 4) positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as a top surface of said substrate, said isolation element partially surrounding the aforementioned first region (cf. column 5, lines 8-13), said isolating element also terminating above a bottom surface of said substrate (see Figure 14).

In conclusion: Chang et al anticipate claim 17.

With regard to claim 18: said isolating element as taught by Chang et al comprises a dielectric material (cf. column 3, lines 7-9).

With regard to claim 19: said isolating element as taught by Chang et al is explicitly allowed to comprise polycrystalline silicon (cf. column 3, lines 7-13).

With regard to claim 21: the first region as taught by Chang et al comprises a power transistor (cf. column 4, lines 41-45), while it is understood by anyone of ordinary skills in the art that any power transistor should be able to control any load, i.e., any impedance including inductive load, as described in standard text books such as B. Jayant Baliga, "Modern Power Devices", Krieger Publishing Co., Malabar, Florida, reprint edition 1992, page 377.

With regard to claim 22: Chang et al teach (cf. Figure 7) an integrated structure (cf. title) comprising:

a substrate 10 (cf. column 4, lines 24-27) having first conductivity type (N+);

an epitaxial layer 20 (cf. column 4, lines 24-27) on said substrate having first conductivity type (N-) and conductivity less than said that of said substrate;

first and second regions in said epitaxial layer (any of the P+ regions to the left of 72c and marked 22 and 24 in Figure 1, as first region, and the P-well to the right of 72c in Figure 7 and marked as 38 in Figure 1, as second region, for definiteness), each having a second conductivity type opposite from said first conductivity type (P-type) , said first and

second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and second junctions therewith; and:

an isolation element 72c (cf. column 5, line 4) positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as said substrate. Chang et al teach the integrated structure to be formed on a semiconductor chip with full trench isolation of each portion of the chip (cf. abstract, first sentence), which implies the length of said isolation element to be substantially if not fully equal to the width of the semiconductor chip and dividing the semiconductor chip into two portions each respectively including said first region and said second region.

In conclusion, Chang et al anticipate claim 22.

With regard to claim 23: said isolation element as taught by Chang et al comprises a dielectric material (cf. column 3, lines 7-9).

With regard to claim 24: said isolation element as taught by Chang et al explicitly is allowed to contain polycrystalline silicon (cf. column 3, lines 7-13).

With regard to claim 26: the first region as taught by Chang et al comprises a power transistor (cf. column 4, lines 41-45), while it is understood by anyone of ordinary skills in the art that any power transistor should be able to control any load, i.e., any impedance including inductive load, as described in standard text books such as B.

Jayant Baliga, "Modern Power Devices", Krieger Publishing Co., Malabar, Florida, reprint edition 1992, page 377.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claims 15, 20, and 25*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al (5,757,081). As detailed above Chang et al anticipate claims 12, 17, and 22 (on which claims 15, 20, and 25 respectively depend). Although Chang et al do not necessarily teach the further limitation that the first conductivity type must be P-type conductivity, it is understood by those of ordinary skills in the art that a mere overall change from an original invention from one set of conductivities to the set obtained by flipping all conductivities does not yield an invention that distinguishes over the prior art when the original invention does not.

5. ***Claims 12-13 and 15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada (5,998,822) in view of Endo (5,990,537). Wada teaches (cf. Figure 2D) an integrated circuit (cf. title) comprising:

a substrate 1 having a first conductivity type (P-type) (cf. column 5, lines 9-15);

an epitaxial layer 2 on said substrate and having first conductivity type and a conductivity less than the conductivity of said substrate (cf. column 5, lines 9-15);

a plurality of regions, a forteriori first and second regions 14 (cf. column 6, lines 26-36) in said epitaxial layer, said first and second regions belonging to different memory cells adjacent to each other in a direction parallel to the bit lines (cf. column 4, lines 42-48), each having second conductivity type (N-type) (cf. column 6, lines 26-36) opposite the first conductivity type, said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and second junctions therewith; and

an isolation element or trench 4a (cf. column 5, line 30 – 36) positioned between said first and second regions and extending from the surface of said epitaxial layer 2 at least as far as said substrate (cf. Figure 2D). The purpose of said trench 4a is to electrically isolate (cf. column 4, lines 63-67) said memory cells from each other, hence to reduce current injection through said epitaxial layer from said first region to said second region when the first junction is biased, said isolating element 4a comprising a dielectric material or insulator 5 (cf. column 5, lines 30-36) adjacent said epitaxial layer 2 (cf. Figure 2D).

Furthermore, Wada et al teaches the isolation element or trench to terminate above a bottom surface of the substrate (cf. Figures 2C and 2D).

Wada does not necessarily teach the isolating element 4a also to comprise polycrystalline silicon spaced apart from said epitaxial layer by said dielectric. However, dielectric isolation is standardly enhanced through the filling of trenches for dielectric isolation by shielding material such as polysilicon, as witnessed by Endo et al, who teach (cf. Figure 4) a dielectric trench isolation layer where the trench comprises an inner filling of polycrystalline silicon 45 spaced apart from epitaxial layer 33 (cf. column 4, line 8) by said dielectric material 46 (here made of silicon dioxide; cf. column 5, line 56). This enhancement is an *obvious* improvement, *as* not just electrostatic charges but also electrostatic fields are kept from crossing through the shielding action of the polysilicon filling. *Reasonable expectation of success is ensured* as only a mild variation in the production process taught by Wada is needed: Wada already applied polysilicon filling to another trench array meant to provide dielectric isolation structures or trenches 32 in the direction parallel to the world lines (cf. column 4, lines 37-42). Finally, *the relevant parts of the two inventions* (Wada and Endo et al) *can be readily combined* as only the polysilicon filling aspect of Endo et al is needed to be introduced into the invention by Wada.

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as taught by Wada at the time it was made so as to include polysilicon filling in the dielectric trench isolation as taught by Endo et al.

With regard to claim 13: said isolation elements 4a and 4b together surround active regions (e.g., 2a and 2b), hence isolation element 4a at least partially surrounds said first region.

With regard to claim 15: the first conductivity as taught by Wada is of P type (cf. column 5, line 13).

6. ***Claim 14*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al (5,757,081) in view of Nakagawa (6,239,465 B1). As detailed above, Chang et al anticipate claim 12. Chang et al do not necessarily teach the further limitation of claim 14. However, isolation trenches for the prevention of electrical interference between different portions of the device and with a length substantially equal to the width of the chip are taught by Nakagawa (cf. Figures 5 and 8). Motivation to include the teaching by Nakagawa in this regard in the invention of Chang et al is the purpose for which the trench is made, namely: to prevent a current path between the different portion of the device: that is what (electrical) isolation element means. Combination of the inventions is easily accomplished as no other limitation pertains to the direction along the width of the chip while any part of the chip in Chang et al not provided with the trench isolation is clearly not substantial to the invention, said trench isolation being shown on each and every embodiment. For the above reasons it would have been obvious to improve the invention by Chang et al in accordance with the abovementioned teaching by Nakagawa so as to accentuate the role and function of the isolation element as taught by Chang et al.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
November 12, 2002